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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,473	12/23/2003	Thomas Sean Houlihane	550-499	8029

23117 7590 11/28/2006

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ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 11/28/2006

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/743,473
Filing Date: December 23, 2003
Appellant(s): HOULIHANE, THOMAS SEAN

John R. Lastova
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/14/06 appealing from the Office action mailed 6/15/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

Claims 10, 15, 21, 34, 39, and 45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1-9, 11-14, 16-20, 22-33, 35-38, 40-44, and 46 stand rejected.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner.

The rejection of claims 23-24 under 35 U.S.C. 101 has been withdrawn.

The rejection of claims 1-4, 7, 18, 22-28, 31, 42, and 46 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication U.S. 2004/0111252 to Burgun et al. has been withdrawn.

The rejection of claims 2-4, 23-24, 26-28, and 46 under 35 U.S.C. 102(e) as being anticipated by Nightingale (US 6,876,941) have been withdrawn.

NEW GROUND(S) OF REJECTION

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 22 and 24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Computer programs claimed as computer listings, *per se*, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer that permit the

computer program's functionality to be realized. In contrast, a claimed computer readable medium encoded with a computer program is a computer elements that defines structural and functional interrelationships between the computer program and the rest of the computer that permit the computer program's functionality to be realized, and is thus statutory. Accordingly, it is important to distinguish claims that define descriptive material *per se* from claims that define statutory inventions. See MPEP 2106.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,876,941	Nightingale	04-2005

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5-9, 11-14, 16-17, 19-20, 22, 25, 29-33, 35-38, 40-41, and 43-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Nightingale (US 6, 876,941).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Nightingale teaches (a) receiving the configuration data used to configure the representation of the device (column 3, lines 12-15); and (b) generating the testbench with reference to the configuration data and a first set of templates defining the test environment (column 3, lines 15-20 and Ref. 300).

Regarding claim 5, Nightingale teaches that the representation of the device is provided in a first language type and at said step (b) a part of the testbench defined by a number of the templates in the first set is generated in a second language type different to the first language type (column 6, lines 34-36 and column 11, lines 16-21).

Regarding claim 6, Nightingale teaches that the first language type is a Register Transfer Language (RTL), and the second language type is a High level Verification Language (HVL) (column 6, lines 34-36 and column 11, lines 16-21).

Regarding claim 7, Nightingale teaches that the device is a bus interconnect block (see Figure 1).

Regarding claim 8, Nightingale teaches employing a simulation tool to run a model of the data processing apparatus using the representation of the device and the testbench (column 7, lines 9-13); wherein the first set of templates includes a master template defining a master engine coupled to a bus and operable during running of the model to generate test stimuli for input via the bus to the representation of the device (column 4, lines 10-12).

Regarding claim 9, Nightingale teaches that the master template includes a master monitor operable during running of the model to monitor signals on the bus to which the master engine is coupled (column 2, lines 16-19 and column 12, lines 6-10).

Regarding claim 11, Nightingale teaches that the master template includes a checker operable during running of the model to check that signals at an interface between the master engine and the bus to which the master engine is coupled conform to a protocol for that bus (column 3, lines 33-38).

Regarding claim 12, Nightingale teaches that the master engine is arranged to generate the test stimuli in a random manner (column 20, lines 49-51).

Regarding claim 13, Nightingale teaches employing a simulation tool to run a model of the data processing apparatus using the representation of the device and the testbench (column 7, lines 9-13); wherein the first set of templates includes a slave template defining a slave engine coupled to a bus and operable during running of the model to generate response signals in reply to test stimuli received from the representation of the device (column 4, lines 10-12).

Regarding claim 14, Nightingale teaches that the slave template includes a slave monitor operable during running of the model to monitor signals on the bus to which the slave engine is coupled (column 12, lines 6-10).

Regarding claim 16, Nightingale teaches that the slave template includes a checker operable during running of the model to check that signals at an interface between the slave engine and the bus to which the slave engine is coupled conform to a protocol for that bus (column 3, lines 33-38).

Regarding claim 17, Nightingale teaches that the slave engine is arranged to generate the response signals in a random manner (column 20, lines 49-51).

Regarding claim 19, Nightingale teaches that there are a number of different component types, and the predetermined attributes specified by the configuration data indicate the component type for each of said one or more components (column 4, lines 3-8).

Regarding claim 20, Nightingale teaches that the device is a bus interconnect block, and wherein one of the component types is a master type, and for each of said one or more components which is a master type, the predetermined attributes identify connections to any slave components within said one or more components that that master type component is connected to (column 3, lines 44-50).

Regarding claim 22, Nightingale teaches a computer program product comprising code portions operable to control a computer to perform a method as claimed in claim 1 (column 9, lines 60-67).

Regarding claim 25, Nightingale teaches logic operable to read the configuration data used to configure the representation of the device (column 3, lines 12-15); and generation logic operable to generate the testbench with reference to the configuration data and a first set of templates defining the test environment (column 3, lines 15-20 and Ref. 300).

Regarding claim 29, Nightingale teaches that the representation of the device is provided in a first language type, and during generation of the testbench by the generation logic a part of the testbench defined by a number of the templates in the first set is generated in a second language type different to the first language type (column 6, lines 34-36 and column 11, lines 15-21).

Regarding claim 30, Nightingale teaches that the first language type is a Register Transfer Language (RTL), and the second language type is a High level Verification Language (HVL) (column 6, lines 34-36 and column 11, lines 16-21).

Regarding claim 31, Nightingale teaches that the device is a bus interconnect block (see Fig. 1).

Regarding claim 32, Nightingale teaches a simulation tool operable to run a model of the data processing apparatus using the representation of the device and the testbench (column 7, lines 9-13); wherein the first set of templates includes a master template defining a master engine coupled to a bus and operable during running of the model to generate test stimuli for input via the bus to the representation of the device (column 4, lines 10-12).

Regarding claim 33, Nightingale teaches that the master template includes a master monitor operable during running of the model to monitor signals on the bus to which the master engine is coupled (column 2, lines 16-19 and column 12, lines 6-10).

Regarding claim 35, Nightingale teaches that the master template includes a checker operable during running of the model to check that signals at an interface between the master engine and the bus to which the master engine is coupled conform to a protocol for that bus (column 3, lines 33-38).

Regarding claim 36, Nightingale teaches that the master engine is arranged to generate the test stimuli in a random manner (column 20, lines 49-51).

Regarding claim 37, Nightingale teaches a simulation tool operable to run a model of the data processing apparatus using the representation of the device and the testbench (column 7, lines 9-13); wherein the first set of templates includes a slave template defining a slave engine coupled to a bus and operable during running of the model to generate response signals in reply to test stimuli received from the representation of the device (column 4, lines 10-12).

Regarding claim 38, Nightingale teaches that the slave template includes a slave monitor operable during running of the model to monitor signals on the bus to which the slave engine is coupled (column 12, lines 6-10).

Regarding claim 40, Nightingale teaches that the slave template includes a checker operable during running of the model to check that signals at an interface between the slave engine and the bus to which the slave engine is coupled conform to a protocol for that bus.

Regarding claim 41, Nightingale teaches that the slave engine is arranged to generate the response signals in a random manner (column 20, lines 49-51).

Regarding claim 43, Nightingale teaches that there are a number of different component types, and the predetermined attributes specified by the configuration data indicate the component type for each of said one or more components (column 4, lines 3-8).

Regarding claim 44, Nightingale teaches that the device is a bus interconnect block, and wherein one of the component types is a master type, and for each of said one or more components which is a master type, the predetermined attributes identify connections to any

slave components within said one or more components that that master type component is connected to (column 3, lines 44-50).

(10) Response to Argument

- **Nightingale Does Not Generate the Representation Of The Device Under Test (DUT)**

The rejection of claims 2, 23, 26, and 46 under 102(e) as being anticipated by Nightingale have been withdrawn, therefore this argument is moot.

- **Nightingale Does Not Configure The Representation Of The Device Under Test (DUT) Using The Claimed Configuration Data**

Nightingale teaches a configuration file containing predetermined parameters identifying the type of the device and capabilities of the device (column 3, lines 14-16 and 26-28). The preamble of the claim states that the representation of the device is "configurable based on configuration data specifying predetermined attributes of the one or more components."

Applicant argues that that because the DUT has already been defined, the prior art does not read on the claim. However, the preamble of the claim merely states that the representation of the device is configurable, i.e. able to be modified or arranged or configured, based on the configuration data. It does not claim when the representation of the device must be configured or that it cannot already be configured.

Furthermore, the configuration data contains data "specifying predetermined attributes of one or more components". Clearly the representation of the device has been configured in a way

such that it contains the components defined in the configuration data and that these components are arranged in a way defined in the configuration data. Therefore, it has clearly been configured with respect to the information contained in the configuration file.

- **Nightingale Does Not Describe Generating The DUT Testbench With Reference To The Configuration Data And A First Set Of Templates Defining The Test Environment**

Nightingale teaches generating a test environment for the device by creating selected test components which are coupled via the bus with a representation of the device to form the test environment, the test components being selected dependent upon the configuration file (column 3, lines 16-20). Applicant argues that this configuration file is not the same configuration file used to configure the representation of the device under test. As stated above, the configuration file contains the information used to configure the representation of the device since it contains information about the attributes and components of the DUT. The information in the configuration file, i.e. the components of the DUT and the interconnection of the components, was used in order to arrange or configure the representation of the device. Clearly the representation was configured in order to create an accurate representation of the device. And in order to be configured, a file containing the information about the components in the device and the interconnection of the components was required. The information in this file is the same information found in Nightingale's configuration file since the configuration file contains parameters identifying the type of device and capabilities of the device. Therefore, in

Nightingale, a test environment is created using the information used to configure the representation of the device under test.

Applicant argues that Nightingale does not teach a first set of templates defining the test environment. Nightingale teaches that the configuration engine may have access to a variety of different test components which it can select for inclusion in the test environment dependent on information contained within the configuration file (column 3, lines 42-45). Although the word template is not specifically used, as applicant argues, the configuration engine takes two things into account when creating the test environment: the variety of test components available and the information contained in the configuration file. The variety of different test components that can be used is a model or template for possible components that can make up the environment. Therefore, this "template" is used in conjunction with the information supplied in the configuration data to create the test environment. Therefore, Nightingale reads on the independent claims.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

This examiner's answer contains a new ground of rejection set forth in section **(9)** above. Accordingly, appellant must within **TWO MONTHS** from the date of this answer exercise one

of the following two options to avoid *sua sponte* **dismissal of the appeal** as to the claims subject to the new ground of rejection:

(1) **Reopen prosecution.** Request that prosecution be reopened before the primary examiner by filing a reply under 37 CFR 1.111 with or without amendment, affidavit or other evidence. Any amendment, affidavit or other evidence must be relevant to the new grounds of rejection. A request that complies with 37 CFR 41.39(b)(1) will be entered and considered. Any request that prosecution be reopened will be treated as a request to withdraw the appeal.

(2) **Maintain appeal.** Request that the appeal be maintained by filing a reply brief as set forth in 37 CFR 41.41. Such a reply brief must address each new ground of rejection as set forth in 37 CFR 41.37(c)(1)(vii) and should be in compliance with the other requirements of 37 CFR 41.37(c). If a reply brief filed pursuant to 37 CFR 41.39(b)(2) is accompanied by any amendment, affidavit or other evidence, it shall be treated as a request that prosecution be reopened before the primary examiner under 37 CFR 41.39(b)(1).

Extensions of time under 37 CFR 1.136(a) are not applicable to the TWO MONTH time period set forth above. See 37 CFR 1.136(b) for extensions of time to reply for patent applications and 37 CFR 1.550(c) for extensions of time to reply for ex parte reexamination proceedings.

Respectfully submitted,

msw

11/21/06

John Barlow
Supervisory Patent Examiner
Technology Center 2800

A Technology Center Director or designee must personally approve the new ground(s) of rejection set forth in section (9) above by signing below:

Conferees:

John Barlow

Ricky Mack

Approved.

JANICE A. FALCONE
DIRECTOR
TECHNOLOGY CENTER 2800